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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,929	ORCHARD, JOHN T.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 01 June 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-5 and 7-49 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-5 and 7-49 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

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DETAILED ACTION

1. This communication is responsive to Amendment filed 06/01/2005.

2. Claims 2-5 and 7-49 are pending in this application. Claims 2, 17, 32, and 44 are independent claims. In Amendment, claims 1 & 6 are cancelled and claims 44-49 are added. This Office Action is made non-final after a RCE filed 06/01/2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 2-3, 5, 7-9, 17-18, 20-24, 44-46, and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Grisamore (U.S. 6,535,901).

Re claim 2, Grisamore discloses in Figures 1, 4-5, and 7 an apparatus comprising: a plurality of inputs to receive multiple input terms (e.g. 1st current multiplicand 20 and 2nd current multiplicand 22 in Figure 1); a multi-stage series of Boolean function generators (e.g. 14 and 16 in Figure 1) coupled with the inputs to implement one or more full-adders and associated registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 2 lines 36-40 and col. 3 lines 55-

61), half-adders (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 2 lines 36-40 and col. 3 lines 55-61), and single registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 1 lines 36-38) to produce intermediate summation results (e.g. output of reduction tree module 14 as 1st preceding resultant 26 and 2nd preceding resultant 28) by combining the input terms (e.g. partial product terms from generator 12) according to a pipelined reduction pattern (e.g. col. 1 lines 32-41, col. 2 lines 35-42, and col. 3 lines 20-27), such that input bits of equal significance are partitioned into groups of three to serve as inputs to full-adders (e.g. col. 8 lines 20-33), remaining groups of two to serve as inputs to half-adders (e.g. col. 8 lines 20-33), and remaining single bits to serve as inputs to single registers (e.g. col. 5 lines 48-53); and a multi-input adder (e.g. 18 as adder in Figure 1) logically coupled with the series of Boolean function generators (e.g. reduction tree module 14) to produce a final sum (e.g. multiplied accumulated resultant 34) of the input terms by combining the intermediate summation results (e.g. output of 14).

Re claim 3, Grisamore further discloses in Figures 1, 4-5, and 7 the input terms include one or more accumulator bits (e.g. 26 and 28 wherein each of these bits is the resultant bit of previous or preceding summation).

Re claim 5, Grisamore further discloses in Figures 1, 4-5, and 7 the Boolean function generator pairs with an associated register to form the atomic structure of a dedicated logic device (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 1 lines 36-38).

Re claim 7, Grisamore further discloses in Figures 1, 4-5, and 7 the multi-input adder comprises an adder (e.g. adder 18 in Figure 1) with an input for each single register in a final stage of the multiple stages of the series (e.g. col.3 lines 60-63 and Figure 5 layer 2).

Re claim 8, Grisamore further discloses in Figures 1, 4-5, and 7 single registers in the series of Boolean function generators to receive feedback accumulator bits (e.g. 26 and 28 in Figure 1 and Figure 5 layer 6 as feedback from layer 2) from the multi-input adder, the accumulator bits resulting from a multiply-accumulate operation (e.g. output of 18 in Figure 1).

Re claim 9, Grisamore further discloses in Figures 1, 4-5, and 7 single registers in the series of Boolean function generators to receive feedback accumulator bits (e.g. 26 and 28 in Figure 1 and Figure 5 layer 6 as feedback from layer 2) from the multi-input adder, the accumulator bits resulting from a multiply-accumulate operation (e.g. output of 18 in Figure 1) and an accumulator coupled with the multi-input adder to feed the accumulator bits back into the series of Boolean function generator (e.g. feedback from output of 16 to input of reduction tree module 14 in Figure 1).

Re claim 17, it is a method claim of claim 2. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 18, it is a method claim of claim 3. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 20, it is a method claim of claim 5. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 21, Grisamore further discloses in Figures 1, 4-5, and 7 the intermediate summation results (e.g. output of reduction tree module 14 in Figure 1) comprises combining the input terms (e.g. terms from partial product generator 12, and inputs from 26 and 28 in Figure 1) with a multi-stage series of Boolean function generators structured to receive three-bit input terms by a full-adder (e.g. layer 6 in Figure 5), two-bit input terms by a half-adder (e.g. layer 6 in Figure 5), and single-bit input terms by a single register (e.g. layer 6 in Figure 5 and col. 1 lines 32-41).

Re claim 22, it is a method claim of claim 7. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 23, it is a method claim of claim 8. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 24, it is a method claim of claim 9. Thus, claim 24 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 44, Grisamore discloses in Figures 1, 4-5, and 7 an apparatus (e.g. Figure 1 and abstract) comprising: a summing module generator (e.g. part 14, 16, and 18 in Figure 1), summing module generator being configured to: receive input terms (e.g. 1st current multiplicand 20 and 2nd current multiplicand 22 in Figure 1); perform bit-wise analysis of the input terms (e.g. col. 2 lines 35-40 and col. 3 lines 42-47); and dynamically configure a summing module (e.g. through reduction tree module 14 in Figure 1), wherein the summing module, as configured, comprises: a hybrid Wallace tree comprising one or more elements (e.g. col. 2 lines 62-68), wherein the elements comprise adders with one or more associated registers and one or more other resisters (e.g. col. 1

lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 1 lines 36-38), wherein the Wallace tree is configured to have a reduced number of elements to perform summing operations on the one or more input terms (e.g. col. 1 lines 42-47 and col. 2 lines 62-68); and a multi-input adder (e.g. adder 18 in Figure 1) configured to combine summation results produced by the configured summing module.

Re claim 45, Grisamore further discloses in Figures 1, 4-5, and 7 the adders comprise one or more full-adders and one or more half-adders (e.g. col. 3 lines 42-47).

Re claim 46, it is an apparatus claim of claim 3. Thus, claim 46 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 49, the hybrid Wallace tree is dynamically configured, wherein the configurations based at least in part on one or more properties of the input terms (e.g. col. 3 lines 42-49).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 10-12, 19, 25-27, and 47-48 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs").

Re claim 4, Grisamore does not disclose the Boolean function generator comprise four-input look-up tables (LUTs) to implement Boolean logic functions. However, Chang et al. disclose in Figure 1(a) Boolean function generator comprise four-input look-up tables (LUTs) to implement Boolean logic functions (e.g. left column page 310 lines 1-5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a LUTs to implement Boolean logic functions as seen in Chang's invention into Grisamore's invention because it would enable to reduce the hardware cost (e.g. introduction section on page 309 lines 7-15).

Re claims 10-12, Grisamore does not disclose in Figures 1, 4-5, and 7 the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA and a device with control logic and a block of dedicated logic. However, Chang et al. disclose the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA (e.g. 2nd paragraph on the left column page 309) and a device with control logic and a block of dedicated logic (e.g. control signals for controlling the block of hardware. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to implement the Boolean function generators in a dedicated logic device comprising a FPGA with control logic and a block of dedicated logic as seen in Chang et al.'s invention into Grisamore's invention because it would enable to reduce the hardware cost for performing logic functions (e.g. 2nd paragraph on the left column page 309).

Re claim 19, it is a method claim of claim 4. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 25, it is a method claim of claim 10. Thus, claim 25 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 26, it is a method claim of claim 11. Thus, claim 26 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 27, it is a method claim of claim 12. Thus, claim 27 is also rejected under the same rationale in the rejection of rejected claim 12.

Re claim 47, it is an apparatus claim of claim 10. Thus, claim 47 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 48, it is an apparatus claim of claim 11. Thus, claim 48 is also rejected under the same rationale in the rejection of rejected claim 11.

7. Claims 13-16 and 28-31 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs"), as applied to claims 1, 10, and 25 above, in view further of Fang et al. ("A hierarchical functional structuring and partitioning approach for multiple-FPGA implementations").

Re claims 13-16, Grisamore in view of Chang disclose in Figures 1, 4-5, and 7 an FPGA architecture to implement the one or more full-adders (e.g. Figure 3), half-adders (e.g. Figure 2), and single registers (e.g. col. 1 lines 35-40 and col. 3 lines 42-48), the architecture based at least in part on an analysis of the input terms (e.g. col. 2 lines 35-40) comprising a bit-wise analysis (e.g. col. 2 lines 33-35). Grisamore in view of Chang do not disclose in Figures 1, 4-5, and 7 a controller or a logic control module dynamically

structures the atomic elements of the dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically (e.g. left column 3rd paragraph page 1189 and Module1(DP) in Figure 3 and Figure 1) structures the atomic elements of the dedicated logic device (e.g. Figure 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device as seen in Fang's invention into Grisamore in view of Chang's invention because it would enable an operator to dynamically program or configure a specific function in low manufacturing time and cost (e.g. first paragraph in the introduction section).

Re claim 28, it is a method claim of claim 13. Thus, claim 28 is also rejected under the same rationale in the rejection of rejected claim 13.

Re claim 29, it is a method claim of claim 14. Thus, claim 29 is also rejected under the same rationale in the rejection of rejected claim 14.

Re claim 30, it is a method claim of claim 16. Thus, claim 30 is also rejected under the same rationale in the rejection of rejected claim 16.

Re claim 31, it is a method claim of claim 15. Thus, claim 31 is also rejected under the same rationale in the rejection of rejected claim 15.

8. Claims 32, 36-38, and 42-43 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979).

Re claim 32, Grisamore discloses in Figures 1, 4-5, and 7 a method for performing arithmetic comprising: generating a plurality of partial products from two or more input terms (e.g. partial product generator 12 in Figure 1); that implements in one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results by combining the partial products (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and col. 2 lines 35-40); determining the structure of the Boolean function generators based, at least in part, on one or more attributes of the input terms (e.g. col. 8 lines 20-30); receiving in both branches accumulator bits over a feedback path (e.g. 26 and 28); and adding (e.g. adder 18 in Figure 1) the intermediate summation results with the accumulator bits for each branch to produce a final components sum (e.g. output of adder 18 in Figure 1). Grisamore does not implicitly disclose two paths one for a real-component branch, inverting certain partial products and passing the inverted and non-inverted partial products and one for an imaginary-component branch, passing the partial products to a multi-stage series of Boolean function generators simultaneously. However, Greenberger clearly discloses in Figure 2 a complex arithmetic operation comprising two paths (e.g. real and imaginary wherein label with Zr and Zi) one for a real-component branch (e.g. left side of Figure 2) inverting certain partial products (e.g. 34.1 for subtraction) and passing the inverted and non-inverted partial products and one for an imaginary-component branch (e.g. right side of Figure 2), passing the partial products (e.g. 34.2 for addition). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add two paths one for

a real-component branch, inverting certain partial products and passing the inverted and non-inverted partial products and one for an imaginary-component branch, passing the partial products as seen in Greenberger's invention into Grisamore's invention because it would enable to reduce the complexity of processing the complex operands and the area in an integrated circuit (e.g. col. 3 lines 38-42 and col. 4 lines 45-52).

Re claim 36, Grisamore further discloses in Figures 1, 4-5, and 7 generating a plurality of partial product terms comprises combining the two or more inputs in a combinatorial stage of a complex multiply accumulator (e.g. Figure 1 as multiplication).

Re claim 37, Grisamore further discloses in Figures 1, 4-5, and 7 analyzing one or more attributes of the input terms (e.g. col. 2 lines 35-40).

Re claim 38, Grisamore further discloses in Figures 1, 4-5, and 7 analyzing the one or more attributes of the input terms comprises performing a bit-wise analysis of the input terms (e.g. col. 2 lines 33-35 wherein the bit-wise is logical function of the partial products).

Re claim 42, Grisamore further discloses in Figures 1, 4-5, and 7 the multi-stage series of Boolean function generators are pipelined (e.g. Figure 5 wherein the reduction stage goes from high to low; e.g. 6, 4, 2... and col. 1 lines 32-41).

Re claim 43, Grisamore further discloses in Figures 1, 4-5, and 7 the partial products of the two or more input terms are reduced according to a pattern structured (e.g. col. 2 lines 35-43) by partitioning bits of equal significance into groups of three to be passed as inputs to the full-adders, remaining groups of two to be passed ms inputs to

the half-adders (e.g. col. 8 lines 20-30), and remaining single bits to be passed to single registers (e.g. col. 5 lines 48-53).

9. Claims 33-35 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979), as applied to claim 32 above, in further view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs").

Re claims 33-35, Grisamore in view of Greenberger do not disclose in Figures 1, 4-5, and 7 the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA and a device with control logic and a block of dedicated logic. However, Chang et al. disclose the series of Boolean function generators is incorporated in a dedicated logic device comprising a FPGA (e.g. 2nd paragraph on the left column page 309) and a device with control logic and a block of dedicated logic (e.g. control signals for controlling the block of hardware. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to implement the Boolean function generators in a dedicated logic device comprising a FPGA with control logic and a block of dedicated logic as seen in Chang et al.'s invention into Grisamore in view of Greenberger's invention because it would enable to reduce the hardware cost for performing logic functions (e.g. 2nd paragraph on the left column page 309).

10. Claims 39-41 are rejected under 35 U.S.C. 103(a) as being obvious over Grisamore (U.S. 6,535,901) in view of Greenberger (U.S. 6,411,979) in further view of Chang et al. ("Hardware-

efficient implementations for discrete function transforms using LUT-based FPGAs"), as applied to claim 37 above, and in further view of Fang et al. ("A hierarchical functional structuring and partitioning approach for multiple-FPGA implementations").

Re claims 39-41, Grisamore in view of Greenberger in further view of Chang et al. disclose in Figures 1, 4-5, and 7 a dedicated logic architecture to implement the one or more full-adders (e.g. Figure 3), half-adders (e.g. Figure 2), and single registers (e.g. col. 1 lines 35-40 and col. 3 lines 42-48), the architecture based at least in part on an analysis of the input terms (e.g. col. 2 lines 35-40) comprising a bit-wise analysis (e.g. col. 2 lines 33-35). Grisamore in view of Greenberger in further view of Chang et al. do not disclose in Figures 1, 4-5, and 7 a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device. However, Fang et al. disclose in Figure 3 a controller or a logic control module dynamically (e.g. left column 3rd paragraph page 1189 and Module1(DP) in Figure 3 and Figure 1) structures the atomic elements of the dedicated logic device (e.g. Figure 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a controller or a logic control module dynamically structures the atomic elements of the dedicated logic device as seen in Fang's invention into Grisamore in view of Greenberger in further view of Change et al.'s invention because it would enable an operator to dynamically program or configure a specific function in low manufacturing time and cost (e.g. first paragraph in the introduction section).

Response to Arguments

11. Applicant's arguments filed 06/01/2005 have been fully considered but they are not persuasive.

a. The applicant argues in page 12 second paragraph for claims rejected under 35 U.S.C. 102(e) that the cited reference by Grisamore does not disclose one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results as cited in the claimed invention.

The examiner respectfully submits that Grisamore does disclose one or more full-adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results as clearly addressed in the rejection above. As indicated in col. 1 lines 32-41, col. 3 lines 19-27, and col. 6 lines 60-68, during pipelining there must be associated registers to store the partial results of each adder before loading into the next stage of pipeline wherein the associated registers and single registers are registers at optimal points in the array multiplier. Having these registers in multiplication pipelining would enable to efficiently perform calculation.

b. The applicant argues generally in pages 13-15 for other claims rejected under 35 U.S.C. 103(a) that the cited reference(s) fails to recite a multi-state series of Boolean function generators coupled with the inputs to implement one or more full adders and associated registers, half-adders and associated registers, and single registers to produce intermediate summation results.

The examiner respectfully submits that similarly response to this argument is cited above. In addition, the secondary reference by Chang et al. discloses in Figure 1(a) multi-state series of Boolean function generator comprise four-input look-up tables (LUTs) to implement Boolean logic functions (e.g. left column page 310 lines 1-5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a LUTs to implement Boolean logic functions as seen in Chang's invention into Grisamore's invention because it would enable to reduce the hardware cost (e.g. introduction section on page 309 lines 7-15) as clearly addressed in the rejection above.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

c. U.S. Patent No. 5,103,419 to Toyokura et al. disclose a circuit for calculating the sum of products of data.

d. U.S. Patent No. 6,490,608 to Zhu discloses a fast parallel multiplier implemented with improved tree reduction schemes.

e. U.S. Patent No. 4,887,233 to Cash et al. disclose pipeline arithmetic adder and multiplier.

f. U.S. Patent No. 6,883,011 to Rumynin et al. disclose a parallel counter and a multiplication logic circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

August 17, 2005